REMARKS

This is in response to the non-final Official Action currently outstanding with regard to the above-identified application.

Claims 1-24 were pending in this application at the time of the issuance of the currently outstanding Official Action. By the foregoing Amendment, Claims 10 and 22 have been amended. No claims have been cancelled and no claims have been added. Accordingly, Claims 1-24 as hereinabove amended will constitute the claims pending in this application upon the entry of the foregoing Amendment.

In the currently outstanding Official Action, the Examiner has:

1. Acknowledged Applicants claim for foreign priority under 35 USC 119(a)-(d) or (f), and **but still failed to acknowledge the receipt of the required certified copies of the priority documents for this application by the United States Patent and Trademark Office – appropriate confirmation of the receipt of the priority document for this application in response to this communication is respectfully requested;**

2. Provided Applicants with a copy of the Form PTO-1449 that accompanied their Information Disclosure Statement of October 6, 2003 duly signed, dated and initialed by the Examiner in confirmation of his consideration of the art listed therein, **but still failed to provide Applicants with a copy of the Form PTO-1449 that accompanied their Information Disclosure Statement of September 25, 2003 duly signed, dated and initialed by the Examiner to confirm his consideration of the art listed therein – appropriate confirmation of the receipt and consideration of Applicants' Information Disclosure Statement of September 25, 2003 in response to this communication is respectfully requested**;

3. Indicated that the drawings filed as part of this application are objected to on the basis that Figures 3 and 4 should be designated by a legend such as – PRIOR ART --, since only that which is old is illustrated therein – **Applicant respectfully requests that the foregoing Request for Drawing Change Approval be granted and that the new formal drawings submitted concurrently herewith be entered into this case in substitution for the corresponding sheets of drawing as originally filed in response to the Examiner's objection**;

4. Rejected Claims 10 and 22-24 under 35 USC 112 on the basis that the phrase "if the number of tones" is indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention;

5. Rejected Claims 1 and 2 under 35 USC 102(e) as being unpatentable over US Patent 6,426,670 to Tanaka;

6. Rejected Claim 5 and 6 under 35 USC 102(e) as being unpatentable over US Patent 6,549,196 to Taguchi, et al;

7. Rejected Claim 3 under 35 USC 103(a) as being unpatentable over the combination of the Tanaka reference and US Patent 6,580,359 to Tam;

8. Rejected Claims 7 and 8 under 35 USC 103(a) as being unpatentable over the Taguchi, et al reference;

9. Rejected Claim 4 under 35 USC 103(a) as being unpatentable over the Tanaka reference in view of the Tam reference further in view of the Taguchi, et al reference;

10. Rejected Claim 9 on the same grounds as the rejection of Claims 2-8;

11. Rejected Claims 11 and 13 on the same grounds as the rejection of Claims 1-4 with reference to the Taguchi et al Figure 4 as demonstrating how the signal circuit is incorporated into the matrix display;

12. Rejected Claims 12, 14, 16, 18 and 21 apparently under 35 USC 103(a) based upon his previous rejections and an assertion that power savings advantages would have made it obvious to one skilled in the art to include the claimed display circuit in a portable device of the type known in the art;

13. Rejected Claim 15 on the same grounds as stated with respect to Claims 5 and 6 in view of the disclosure in Taguchi et al of how to incorporate the signal circuit into the matrix display;

14. Rejected Claim 17 on the same grounds as stated with respect to Claims 7 and 8 in view of the disclosure in Taguchi et al of how to incorporate the signal circuit into the matrix display;

15. Rejected Claim 19 on the same grounds as stated with respect to Claim 9 in view of the disclosure in Taguchi et al of how to incorporate the signal circuit into the matrix display;

16. Presumably rejected Claims 22-24 on similar grounds as those previously stated, although failing to specifically so state;

17. Indicated that Claim 20 would be allowable if rewritten in independent form including all of the limitations of its base claim and any intervening claims; and

18. Cited certain prior art as being similar to Applicants Disclosure, but failed to apply that art against any of the claims.

With respect to items 1-3 and 17, Applicant respectfully submits that no further comment in these Remarks is required.

With respect to item 4, Claims 10 and 22 have been amended by the foregoing Amendment so as to change the phrase "if the number of tones..." to "*when* the number of tones ...". Applicant respectfully submits that these amendments remove the basis for the Examiner's rejection of Claims 10 and 22-24 under 35 USC 112 as being indefinite. A decision so holding in response to this communication is respectfully requested.

Summarily stated, Applicants' response to the currently outstanding substantive rejections of the claims of the above-identified application is that (i) the references when considered in detail do not support the Examiner's characterizations of them, and/or (ii) the references are insufficient to establish the *prima facie* case of unpatentability that the Examiner is required to supply in support of rejections. In this regard, it will be understood that the present invention has the objectives of reducing power consumption in a signal line drive circuit without adverse impact upon the operating characteristics thereof; providing an image display device that utilizes that signal line drive circuit, and providing portable apparatus utilizing that signal line drive circuit.

To accomplish these objectives, the present invention (i) eliminates an unnecessary circuit from prior art configurations, (ii) eliminates the current that would otherwise be used in the eliminated circuit, and (iii) avoids the occurrence of charging/discharging stray capacitance between bus lines when the image signal represents a small number of tones.

Applicants respectfully submit, on the other hand, that the cited references are taken from totally different technical fields relative to the technical field of the present invention and/or do not either alone or in combination with one another teach, disclose or suggest the present invention as a means of accomplishing the above-stated objectives. Accordingly, for these reasons (as more fully set forth in detail below), Applicant respectfully submits that the currently outstanding rejections of the claims of this application should be withdrawn, and that Claims 1-24 should be allowed.

A main feature of the invention according to claim 1 is *to include a reference voltage line directly inputting (directly transmitting) a first reference voltage* supplied by external reference voltage supply means *to a reference voltage chooser circuit*. With that arrangement, no buffer circuit is required for the reference voltage line directly transmitting the first reference voltage. Therefore, the signal line drive circuit takes up a smaller area and eliminates the amount of current that would otherwise be utilized by a buffer circuit. This results in power savings by the claimed signal line drive circuit in comparison to the prior art.

A main feature of the present invention according to claim 2 is that a second reference voltage produced by voltage division from at least two first reference voltages are supplied to the reference voltage chooser circuit via a buffer circuit having a high input impedance and a low output impedance, *the first reference voltages are directly inputted (directly transmitted) to the reference voltage chooser circuit*, and the reference voltage chooser circuit chooses input voltages in accordance with the tones represented by the image signal and thereafter outputs the chosen voltages as a signal line drive signals. Hence, a main feature of claim 11 is to include the foregoing features of Claim 2 in a display device.

In both cases, no buffer circuits are required for the reference voltage lines directly transmitting the first reference voltages to the reference voltage chooser circuit. Thus, in a manner similar to Claim 1, the signal line drive circuit occupies a smaller area and eliminates the amount of current that otherwise would be expended in a buffer circuit. Again a power saving in the signal line drive circuit is the result.

A main feature of the invention according to claim 3 is that a second reference voltage produced by voltage division from at least two of the first reference voltages is supplied to the reference voltage chooser circuit via a buffer circuit having a high input impedance and a low output impedance, ***a power supply voltage is supplied to the buffer circuit via a first switch controlled by a first control signal***, and the reference voltage chooser circuit chooses input voltages in accordance with the tones represented by the image signal and thereafter outputs the chosen voltages as the signal line drive signals. A main feature of claim 13 is to include the foregoing features of Claim 3 in a display device. Again, in either of these cases, it is possible to eliminate the amount of current that would otherwise occur in the buffer circuit not being used and thereby to realize power savings in the signal line drive circuit.

A main feature of claim 5 is that ***a second switch controlled by a second control signal is provided between a reference voltage lines supplying the first reference voltages and the voltage divider circuit that produces a second reference voltage*** by voltage division from at least two of the first reference voltages. Claim 15 embodies these features in a display device. Here again it is possible to eliminate an amount of current that would otherwise occur in the portion of a prior art voltage divider circuit that is not being used in the present invention thereby realizing a power savings in the signal line drive circuit.

A main feature of claim 7 is that *a decoder circuit* controlling the reference voltage chooser circuit *is controlled through a third control signal to change a decoder table*, whereby the reference voltage chooser circuit changes a reference voltage choosing pattern. Claim 17 carries these features into a display device. In either case, however, the decoder table can be changed in accordance with the number of tones represented by the image signal. Consequently, the signals transmitted by the bus lines are fixed when the image signal represents a small number of tones. This fixation prevents the occurrence of the charging/discharging of stray capacitances between the bus lines thereby also reducing the power consumption of the signal line driving circuit.

Claims 9 and 10 represent combinations of the invention according to claims 3, 5 and 7. Similarly, Claims 19 and 22 represent combinations of the inventions according to Claims 13, 15 and 17. Therefore, it will be readily recognized that the inventions according to claims 9, 10, 19 and 22 also produce the effects just discussed according to the particular combinations of features embodied thereby.

With this summary of the present invention, including its various inherent aspects, Applicants respectfully submit that a suitable frame of reference is established for the consideration of the disclosures of the art relied upon by the Examiner in the currently outstanding Official Action, and for the consideration of the propriety of the Examiner's rejections under appropriate legal standards.

Taking the Tanaka (U.S. Patent No. 6,426,640) reference first, it will be recognized that the objective of that reference is to provide a power circuit that (i) improves the capability of removing noise components from an output voltage, (ii) enhances a driving power to a highly capacitive load, and (iii) achieves a reduction in power consumption while attaining the first two objectives. Applicants, therefore, respectfully submit that the Tanaka reference belongs to a technical field totally different from that of the signal line drive circuits and other circuits according to the present invention, and that one of ordinary skill in the art would not look to the Tanaka reference to achieve the goals of the present invention. Accordingly, it will be recognized that the Tanaka reference does not include all of the elements of the present claims functioning together in the manner claimed, and does not itself, nor in combination with any of the other cited art, teach, disclose or suggest the present invention absent reference to Applicants' disclosures. Of course, to support claim rejections based upon the Tanaka reference it would have to be shown that the Tanaka patent itself disclosed all of the claimed features of the present invention functioning together in the manner claimed, or that the Tanaka reference alone or in combination with the other cited art teaches, discloses or suggests the present invention within its "four corners" without reference to the Applicants' disclosure. Hence, Applicant respectfully submits that the Examiner's rejections based upon the Tanaka reference must fail.

More particularly, it is respectfully noted that the power circuit of the Tanaka reference adopts an arrangement in which a first switching element is provided between a first voltage supply and an output terminal of the power circuit, a second switching element is provided between a second voltage supply and the output terminal, and the second switching element is turned on only to raise an output voltage. Also, reduction in the consumption of power in the circuit is realized in such a manner that the first switching element and the second switching element are controlled so that they are not conductive simultaneously.

In other words, Tanaka merely discloses that either one of the first voltage supply and the second voltage supply is connected to the output terminal. Specifically, the second switching element is turned on to raise (control) the output voltage. Further, either the first voltage supply or the second voltage supply is turned on to prevent to occurrence of a flow-through current between the first and second voltage supplies. Accordingly, as mentioned above, the Tanaka reference belongs to a different technical field from that of the present invention, and discloses, teaches or suggests no technical idea concerning the elimination of an unnecessary circuit to reduce power consumption. In addition, the Tanaka reference fails to disclose components corresponding to all of the components of the present invention (such as, for example, a signal line drive circuit) as would be required to support a valid rejection based upon anticipation under 35 USC 102

The Taguchi, et al reference (U.S. Patent No. 6,549,196), on the other hand, relates to a D/A conversion circuit for driving signal lines inside a pixel array substrate such as a liquid crystal display panel and a liquid crystal display device including that D/A conversion circuit. Further, the objective of the Taguchi et al reference is to suppress fluctuation of an output voltage of a reference power supply such that D/A conversion can be performed at high speed with high precision. Accordingly, Applicants respectfully submit that the Taguchi et al reference's D/A conversion circuit is directed to a totally different objective with a totally different set of problems to be overcome than the signal line drive circuit and other circuits according to the present invention. Hence, the Taguchi et al reference fails to anticipate the present invention under the standards necessary to such a finding under 35 USC 102, and also fails to teach, disclose or suggest the present invention in the manner required to establish unpatentability under 35 USC 103.

In particular, the D/A conversion circuit of the Taguchi et al reference adopts the arrangement of providing a pre-buffer for outputting a voltage substantially equal to an output voltage of a reference power supply and supplying a voltage from the pre-buffer to an output buffer only during a predetermined period of time after a signal from a decoder varies. Alternatively, the Taguchi et al reference provides an arrangement wherein a resistance type voltage divider circuit is provided for charging/discharging the current of an input parasitic capacitor, and other arrangements. With these arrangements, the current charged/discharged from the input parasitic capacitor of the output buffer flows to a charging/discharging voltage generating circuit such as a pre-buffer and resistance type voltage divider circuit without flowing to the reference power supply. The result is a suppression of the fluctuation of the output voltage of the reference power supply. In short, the Taguchi et al reference merely discloses technology for suppressing fluctuations in the output voltages of a reference power supply.

It also is recognized that the Taguchi et al reference discloses a D/A conversion circuit that is provided with switches SW11 through SW18, and three types of current changeover switches SW1 through SW3. It is respectfully noted in this regard, however, that the switches SW11 through SW18 are for dividing the output of the reference power supply so as to select the voltages to be supplied to the output buffer. Further, the current changeover switches SW1 through SW3 are provided for selecting one of the voltages divided from the output voltage and a voltage from the pre-buffer as a voltage to be supplied to the output buffer. In other words, the switches provided in the D/A conversion circuit of the Taguchi et al reference are not provided for eliminating an amount of current that would otherwise occur in a circuit that is not being used in their arrangement. Rather, those switches are provided for selecting (switching) the voltage to be supplied to the output buffer.

Still further, it is to be recognized that the Taguchi et al reference contains no description concerning the number of tones represented by the pixel data, and gives no consideration to the operation of a decoder provided in the disclosed D/A conversion circuit. Accordingly, the Taguchi et al reference cannot be fairly relied upon as teaching, disclosing or suggesting the presently claimed decoder table.

Consequently, Applicants respectfully submit that the Taguchi et al reference has an objective totally different from that of the present invention, and cannot fairly be said to teach, disclose or suggest the technical ideas of (i) eliminating the amount of current that would otherwise occur in a circuit not being used in their arrangement, or (ii) avoiding the occurrence of charging/discharging stray capacitance between the bus lines when the image signal represents a small number of tones with its corresponding reduction in power consumption. Further, Taguchi et al fails to disclose all of the elements of the present invention co-operating with one another in the manner claimed.

Finally, the Tam reference (U.S. Patent No. 6,580,351) relates to a selectable input buffer control system. In particular, Tam discloses a crosspoint switch 10 in which a plurality of input cells 22 are arranged in a matrix manner. However, the crosspoint switch 10 is for selecting signals received from the selectable input buffer control system 12 to output the selected signals to output buffers 82, 84, 86 and 88 (see, column 4, lines 18-25). In other words, the crosspoint switch 10 in the Tam reference is not provided for eliminating the amount of current that would occur in a circuit not being used in the arrangement disclosed, but rather is merely for selecting (switching) signals to be outputted to the output buffers 82, 84, 86 and 88.

Therefore, Applicants respectfully submit that the selectable input buffer control system of the Tam reference has an arrangement that is totally different from that of the signal drive circuit and other circuits of the present invention. In addition, it is noted that the Tam reference contains no description concerning the number of tones represented by the pixel data. Further, the Tam reference contains no teaching, disclosure or suggestion of eliminating the current in a circuit that is not being used as in the present invention.

With respect to anticipation, the law is clear that "a claim is anticipated only if each and every element as set forth in the claim is found either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Company of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) The identical invention must be shown in as complete detail as contained in the...claim. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) The elements must be arranged as required by the claim... *In re Bond,* 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990) As mentioned above, the cited references do not satisfy these standards because none of them disclose all of the components of the present invention functioning in the same way relative to one another as claimed.

With respect to the Examiner's rejections under Section 103 of Title 35 United States Code, it is settled that:

> To establish a *prima facie* case of obviousness under Section 103, Title 35 United States Code (35 US §103), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2D 1438 (Fed. Cir. 1991).

Hence, the test under 35 USC 103 is not "obvious to try", nor is it whether or not the claimed invention could be assembled utilizing components derived from divergent pieces of prior art (i.e., utilizing the claim as a mosaic into which various divergent elements of the prior art are fit without any suggestion in the art itself to do so).

In view of the above discussion, therefore, Applicants respectfully submit that the currently outstanding rejections are insufficient to preclude the patentability of the claims of this application. Specifically, the claims are not anticipated because all of their elements co-operating with one another in the manner claimed are to be found in the cited art.

Furthermore, the claims are not obvious in view of the cited art because the cited art fails to provide the suggestion or motivation for its combination in the manner herein claimed, it fails to carry any reasonable indication of the success of the claimed combination because it deals with totally different problems in different contexts that that of the present invention, and it does not (absent reference to Applicants' specification) teach or suggest all of the limitations of the present claims as has been demonstrated in detail by the foregoing discussion.

For each and all of the foregoing reasons, Applicants respectfully submit that (i) that the references relied upon by the Examiner when considered in detail do not support the Examiner's characterizations of them, and/or (ii) that the references relied upon by the Examiner are insufficient whether taken alone or in combination with one another to establish a *prima facie* case supporting the Examiner's assertion that the claims currently pending in this application are not patentable. Accordingly, Applicants respectfully submit that this application as it currently stand is in condition for allowance, and respectfully request a decision so holding in response to this communication.

Applicants believe that additional fees are not required for consideration of the foregoing Remarks in support of Applicants' traverse of all of the currently outstanding rejections of the claims of the above-identified application. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

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